// VerilogA for ADC\_Ideal\_10bit\_Pipeline, VerilogA\_1bit\_ADC, veriloga

`include "constants.vams"

`include "disciplines.vams"

module VerilogA\_1bit\_ADC(dout,vout,vdd,vss,vmin,vmax,vin);

parameter real vtrans=0.5;

parameter real delay = 0;

parameter real ttime = 1p;

inout vdd,vss;

input vin;

input vmin, vmax;

output vout,dout;

electrical dout,vout,vdd,vss,vmin,vmax,vin;

real vref,v\_result,d\_result;

analog begin

vref = (V(vmax) - V(vmin))/2;

if(V(vin) > vref) begin

d\_result = V(vdd)/V(vdd);

v\_result = (V(vin) - vref)\*2;

end

else begin

d\_result = 0;

v\_result = (V(vin))\*2;

end

V(vout) <+ transition(v\_result,delay,ttime);

V(dout) <+ transition(d\_result,delay,ttime);

end

endmodule